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## Errata

- Reset During EEPROM Write
- Verifying EEPROM in System

### 2. Reset During EEPROM Write

If reset is activated during EEPROM write the result is not what should be expected. The EEPROM write cycle completes as normal, but the address registers are reset to 0. The result is that both the address written and address 0 in the EEPROM can be corrupted.

#### Problem Fix/Workaround

Avoid using address 0 for storage, unless you can guarantee that you will not get a reset during EEPROM write.

### 1. Verifying EEPROM in System

EEPROM verify in In-System Programming mode cannot operate with maximum clock frequency. This is independent of the SPI clock frequency.

#### Problem Fix/Workaround

Reduce the clock speed, or avoid using the EEPROM verify feature.



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**8-Bit AVR<sup>®</sup>**  
**Microcontroller**  
**with 1K bytes**  
**In-System**  
**Programmable**  
**Flash**

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**AT90S1200/A**  
**Rev. F**  
**Errata Sheet**

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